# NTB23N03R

# Power MOSFET
# 23 Amps, 25 Volts
## N−Channel D²PAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

### Features

- Pb−Free Packages are Available

### Typical Applications

- Planar HD3e Process for Fast Switching Performance
- Low $R_{DS(on)}$ to Minimize Conduction Loss
- Low $C_{iss}$ to Minimize Driver Loss
- Low Gate Charge
- Optimized for High Side Switching Requirements in High−Efficiency DC−DC Converters

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise specified)

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Drain−to−Source Voltage | $V_{DSS}$ | 25 | Vdc |
| Gate−to−Source Voltage − Continuous | $V_{GS}$ | ±20 | Vdc |
| Drain Current<br>− Continuous @ $T_A$ = 25°C, Limited by Chip<br>− Continuous @ $T_A$ = 25°C, Limited by Package<br>− Single Pulse ($t_p$ = 10 μs) | <br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>23<br>6.0<br>60 | A |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 37.5 | W |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | −55 to 150 | °C |
| Thermal Resistance − Junction−to−Case | $R_{\theta JC}$ | 3.3 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

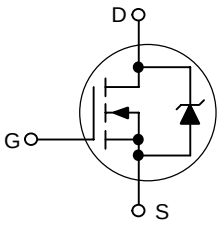
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

**ON Semiconductor®**

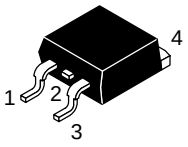
**http://onsemi.com**

**23 AMPERES, 25 VOLTS**
**$R_{DS(on)}$ = 32 mΩ (Typ)**

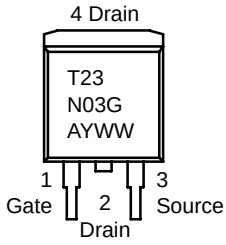
N−CHANNEL




**MARKING DIAGRAM & PIN ASSIGNMENTS**




**D²PAK**
**CASE 418B**
**STYLE 2**




T23N03 = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

© Semiconductor Components Industries, LLC, 2005

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise specified)

| Characteristics | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain−to−Source Breakdown Voltage (Note 1)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V(br)_{DSS}$ | <br>25<br>− | <br>28<br>− | <br>−<br>− | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | <br>−<br>− | <br>−<br>− | <br>1.0<br>10 | μAdc |
| Gate−Body Leakage Current<br>($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | − | − | ±100 | nAdc |
| **ON CHARACTERISTICS** (Note 1) | | | | | | |
| Gate Threshold Voltage (Note 1)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>1.0<br>− | <br>1.8<br>− | <br>2.0<br>− | Vdc<br><br>mV/°C |
| Static Drain−to−Source On−Resistance (Note 1)<br>($V_{GS}$ = 4.5 Vdc, $I_D$ = 6 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 6 Adc) | | $R_{DS(on)}$ | <br>−<br>− | <br>50.3<br>32.3 | <br>60<br>45 | mΩ |
| Forward Transconductance (Note 1)<br>($V_{DS}$ = 10 Vdc, $I_D$ = 6 Adc) | | $g_{FS}$ | <br>− | <br>14 | <br>− | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 V, f = 1 MHz) | $C_{iss}$ | − | 225 | − | pF |
| Output Capacitance | | $C_{oss}$ | − | 108 | − | |
| Transfer Capacitance | | $C_{rss}$ | − | 48 | − | |
| **SWITCHING CHARACTERISTICS** (Note 2) | | | | | | |
| Turn−On Delay Time | ($V_{GS}$ = 10 Vdc, $V_{DD}$ = 10 Vdc, $I_D$ = 6 Adc, $R_G$ = 3 Ω) | $t_{d(on)}$ | − | 2.0 | − | ns |
| Rise Time | | $t_r$ | − | 14.9 | − | |
| Turn−Off Delay Time | | $t_{d(off)}$ | − | 9.9 | − | |
| Fall Time | | $t_f$ | − | 2.0 | − | |
| Gate Charge | ($V_{GS}$ = 4.5 Vdc, $I_D$ = 6 Adc, $V_{DS}$ = 10 Vdc) (Note 1) | $Q_T$ | − | 3.76 | − | nC |
| | | $Q_1$ | − | 1.7 | − | |
| | | $Q_2$ | − | 1.6 | − | |
| **SOURCE−DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On−Voltage | ($I_S$ = 6 Adc, $V_{GS}$ = 0 Vdc) (Note 1)<br>($I_S$ = 6 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | <br>−<br>− | <br>0.87<br>0.74 | <br>1.2<br>− | Vdc |
| Reverse Recovery Time | ($I_S$ = 6 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) (Note 1) | $t_{rr}$ | − | 8.7 | − | ns |
| | | $t_a$ | − | 5.2 | − | |
| | | $t_b$ | − | 3.5 | − | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | − | 0.003 | − | μC |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperatures.

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NTB23N03R | $D^2PAK$ | 50 Units / Rail |
| NTB23N03RG | $D^2PAK$<br>(Pb−Free) | 50 Units / Rail |
| NTB23N03RT4 | $D^2PAK$ | 800 Units / Tape & Reel |
| NTB23N03RT4G | $D^2PAK$<br>(Pb−Free) | 800 Units / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

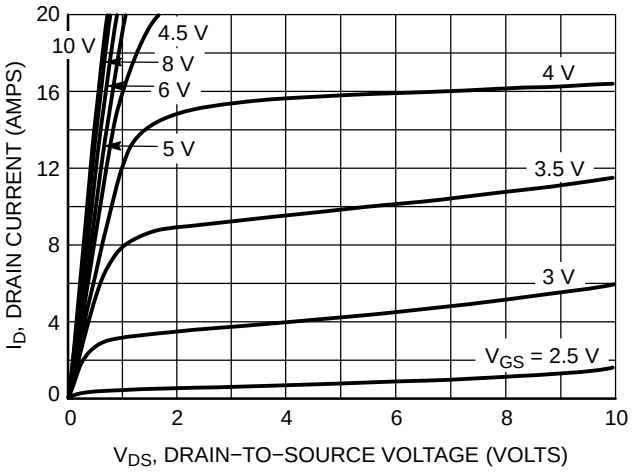



**Figure 1. On−Region Characteristics**

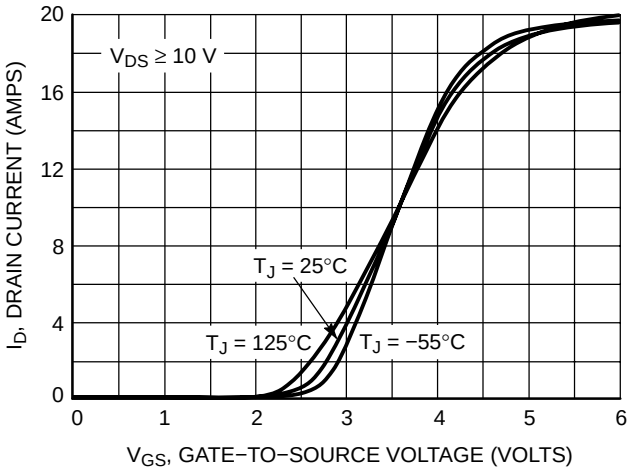



**Figure 2. Transfer Characteristics**

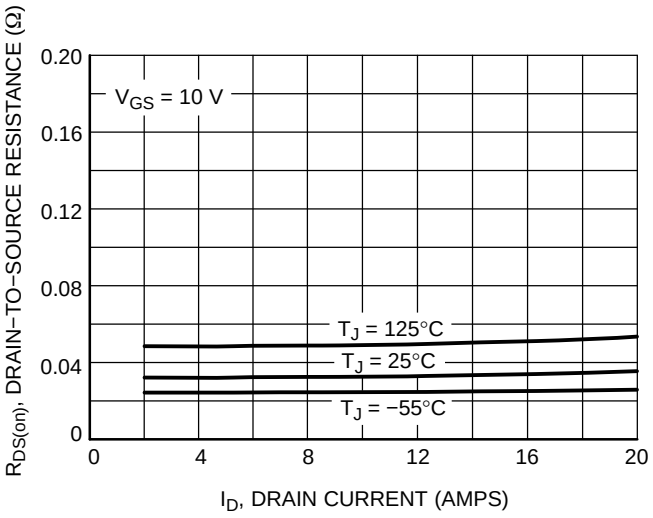



**Figure 3. On−Resistance versus Drain Current and Temperature**

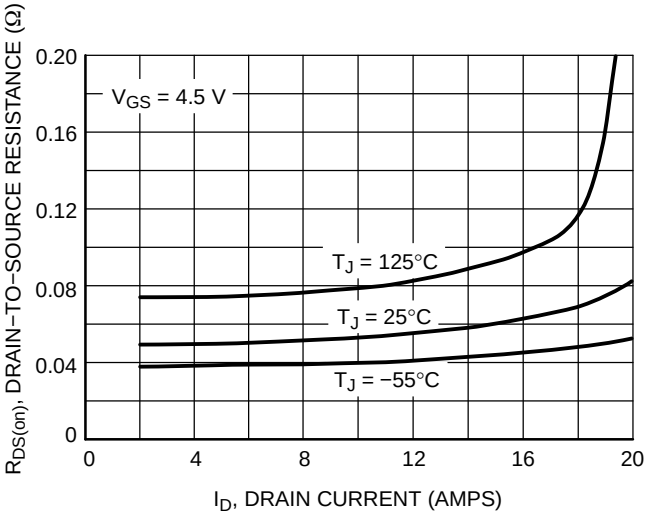



**Figure 4. On−Resistance versus Drain Current and Temperature**

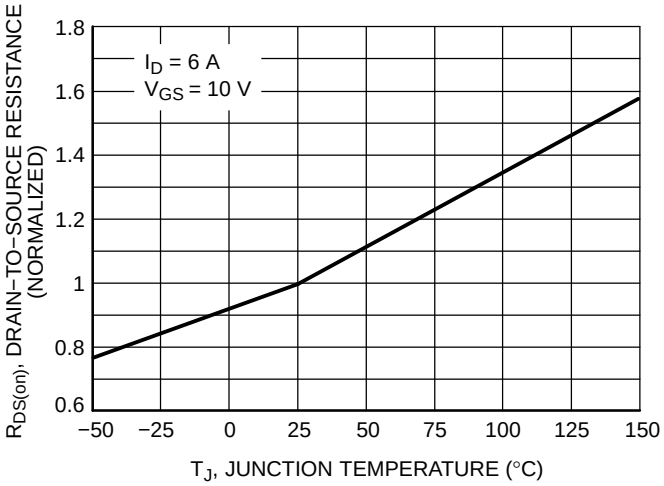



**Figure 5. On−Resistance Variation with Temperature**

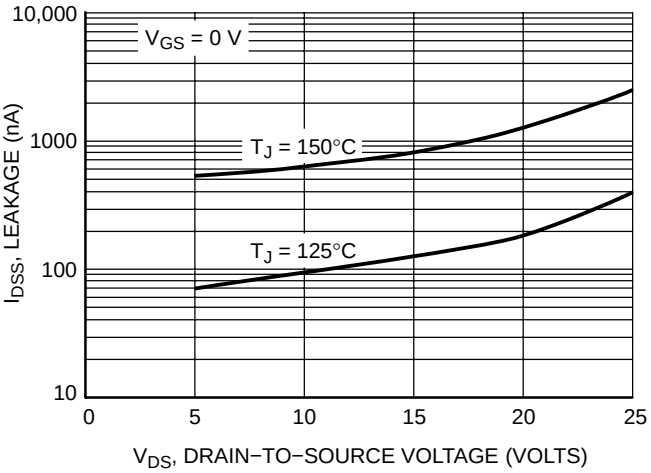



**Figure 6. Drain−to−Source Leakage Current versus Voltage**

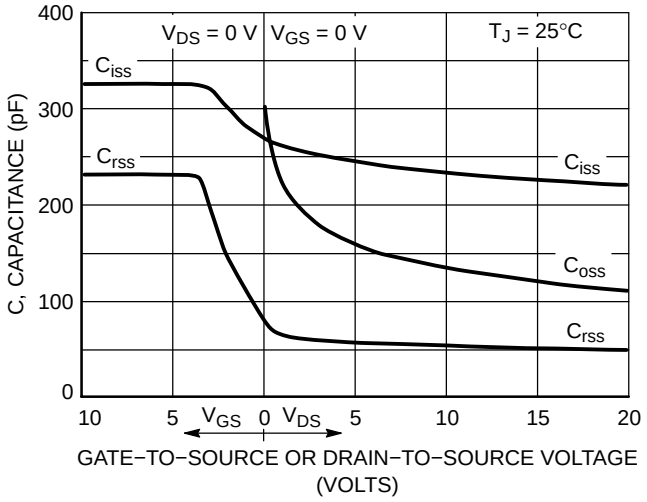



**Figure 7. Capacitance Variation**

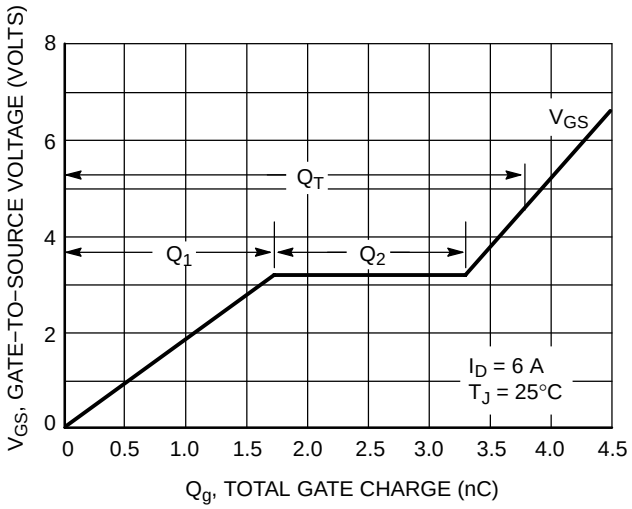



**Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge**

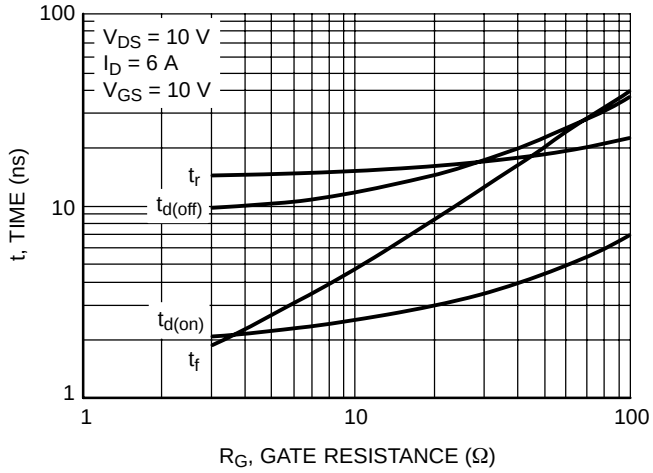



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

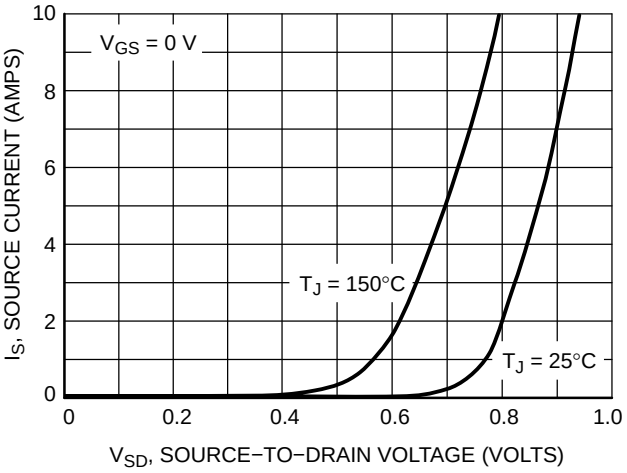
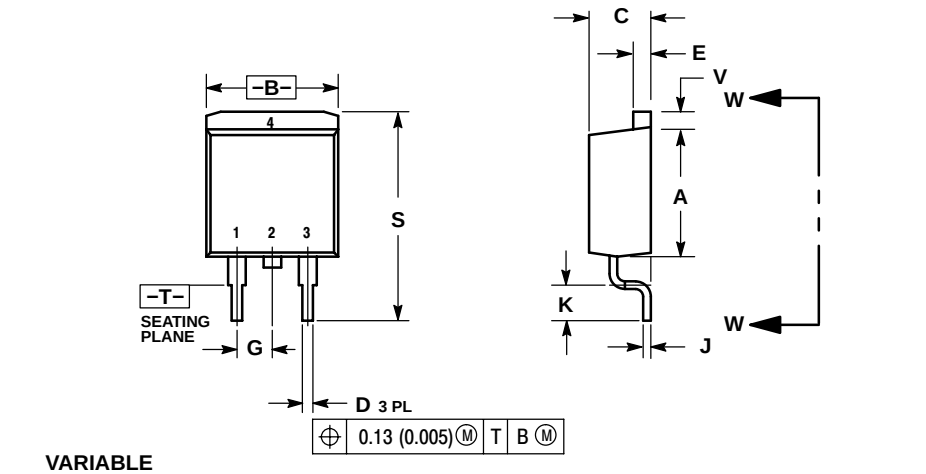



**Figure 10. Diode Forward Voltage versus Current**

## PACKAGE DIMENSIONS

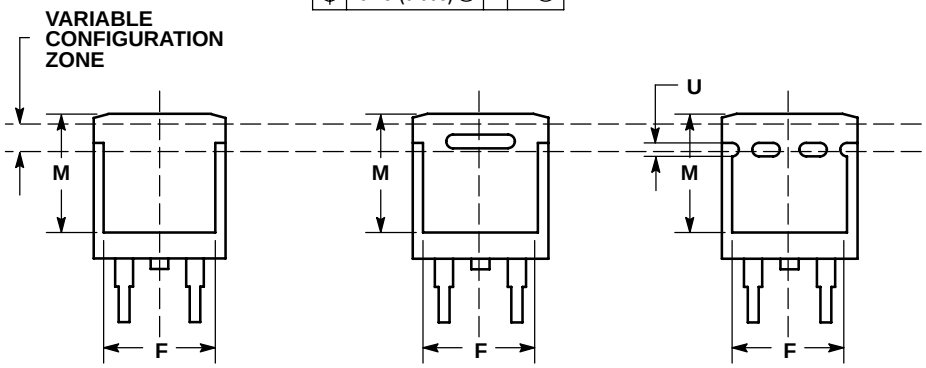
**D²PAK**
CASE 418AA−01
ISSUE O




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

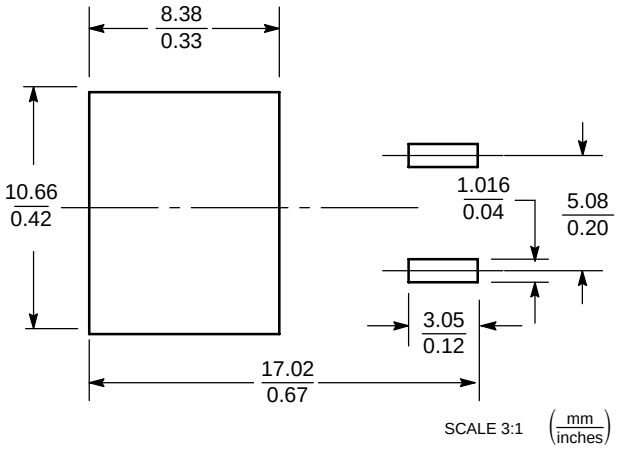
| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.340 | 0.380 | 8.64 | 9.65 |
| B | 0.380 | 0.405 | 9.65 | 10.29 |
| C | 0.160 | 0.190 | 4.06 | 4.83 |
| D | 0.020 | 0.036 | 0.51 | 0.92 |
| E | 0.045 | 0.055 | 1.14 | 1.40 |
| F | 0.310 | −−− | 7.87 | −−− |
| G | 0.100 BSC | | 2.54 BSC | |
| J | 0.018 | 0.025 | 0.46 | 0.64 |
| K | 0.090 | 0.110 | 2.29 | 2.79 |
| M | 0.280 | −−− | 7.11 | −−− |
| S | 0.575 | 0.625 | 14.60 | 15.88 |
| V | 0.045 | 0.055 | 1.14 | 1.40 |

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN




VIEW W−W 1 | VIEW W−W 2 | VIEW W−W 3

### SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**ON Semiconductor** and ON are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT**:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082−1312 USA
**Phone**: 480−829−7710 or 800−344−3860 Toll Free USA/Canada
**Fax**: 480−829−7709 or 800−344−3867 Toll Free USA/Canada
**Email**: orderlit@onsemi.com

**N. American Technical Support**: 800−282−9855 Toll Free USA/Canada

**Japan**: ON Semiconductor, Japan Customer Focus Center
2−9−1 Kamimeguro, Meguro−ku, Tokyo, Japan 153−0051
**Phone**: 81−3−5773−3850

**ON Semiconductor Website**: http://onsemi.com

**Order Literature**: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.